Feng (Dan) Lin's Patent Portfolio

Authors	Patent Title	#	Issued
R. J. Baker, F. Lin	"Digital dual-loop DLL design using coarse and fine loops"	6,445,231	09/03/02
F. Lin	"System and method for skew compensating a clock signal and for capturing a digital signal using the skew compensated clock signal"	6,611,475	08/26/03
F. Lin	"System and method for skew compensating a clock signal and for capturing a digital signal using the skew compensated clock signal"	6,618,283	09/09/03
B. Keeth, B. Johnson and F. Lin	"Method and apparatus for setting and compensating read latency in a high speed DRAM"	6,687,185	02/03/04
F. Lin	"System and method for skew compensating a clock signal and for capturing a digital signal using the skew compensated clock signal"	6,759,882	07/06/04
B. Johnson, B. Keeth and F. Lin	"Method and apparatus for establishing and maintaining desired read latency in high-speed DRAM"	6,762,974	07/13/04
R. J. Baker, F. Lin	"Digital dual-loop DLL design using coarse and fine loops"	6,774,690	08/10/04
F. Lin, R. J. Baker	"Phase detector for all-digital phase locked and delay locked loops"	6,779,126	08/17/04
F. Lin	"System and method to improve the efficiency of synchronous mirror delays and delay locked loops"	6,798,259	09/28/04
F. Lin	"System and method for skew compensating a clock signal and for capturing a digital signal using the skew compensated clock signal"	6,812,753	11/04/04
F. Lin, B. Keeth, B. Johnson	"Method and system for delay control in synchronization circuits"	6,836,166	12/28/04
F. Lin, B. Johnson	"Method and apparatus for improving stability and lock time for synchronous circuits"	6,839,301	01/04/05
F. Lin	"Capture clock generator using master and slave delay locked loops"	6,839,860	01/04/05
F. Lin	"System and method of operation of DLL and PLL to provide tight locking with large range, and dynamic tracking of PVT variations using interleaved delay lines"	6,845,458	01/18/05
F. Lin	"System and method of operation of DLL and PLL to provide tight locking with large range, and dynamic tracking of PVT variations using interleaved delay lines"	6,845,459	01/18/05
F. Lin	"Interleaved delay line for phase locked and delay locked loops"	6,868,504	03/15/05
V. Mikhalev, F. Lin	"Method and apparatus for enabling a timing synchronization circuit"	6,891,415	05/10/05
B. Johnson, F. Lin	"Method and appartus for conpensating duty-cycle distortion in a data output signal from a memory device by delaying and distorting a reference clock"	6,895,522	05/17/05
F. Lin	"Interleaved delay line for phase locked and delay locked loops"	6,912,666	06/28/05
F. Lin, T. Gomm	"Methods and apparatus for delay circuit"	6,930,525	08/16/05
B. Johnson, B. Keeth and F. Lin	"Method and apparatus for establishing and maintaining desired read latency in high-speed DRAM"	6,930,955	08/16/05
F. Lin	"Methods and apparatus for duty cycle control"	6,940,328	09/06/05
F. Lin, R. J. Baker	"Phase splitter using digital delay locked loops"	6,950,487	09/27/05
F. Lin and R. J. Baker	"Phase detector for all-digital phase locked and delay locked loops"	6,987,701	01/17/06
F. Lin	"Circuits and methods of temperature compensation for refresh oscillator"	6,992,534	01/31/06
F. Lin	"Delay lock circuit having self-calibrating loop"	7,009,407	03/07/06
F. Lin	"Interleaved delay line for phase locked and delay locked loops"	7,020,794	03/28/06
B. Johnson, F. Lin	"Duty cycle distortion compensation for the data output of a memory device"	7,028,208	04/11/06

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Authors	Patent Title	#	Issued
B. Keeth, B. Johnson and F. Lin	“Method and apparatus for initialization of read latency tracking circuit in a high speed DRAM”	7,065,001	06/20/06
Feng Lin	“Centralizing the lock point of a synchronous circuit”	7,098,714	08/29/06
F. Lin	“Delay lock circuit having self-calibrating loop”	7,102,361	09/05/06
F. Lin	“Interleaved delay line for phase locked and delay locked loops”	7,103,791	09/05/06
F. Lin	“Phase detector for reducing noise”	7,109,807	09/19/06
F. Lin, R. J. Baker	“Phase detector for all-digital phase locked and delay locked loops”	7,123,525	10/17/06
F. Lin, B. Keeth, B. Johnson, SH. Lee	“Memory system and method for strobing data, command and address signals”	7,126,874	10/24/06
F. Lin, B. Johnson	“Method and apparatus for calibrating driver impedance”	7,129,738	10/31/06
F. Lin	“Phase detector for reducing noise”	7,129,794	10/31/06
F. Lin	“Phase detector for reducing noise”	7,132,898	11/07/06
F. Lin	“Method and apparatus to set a tuning range for an analog delay”	7,138,845	11/21/06
F. Lin, T. Gomm	“Methods and apparatus for delay circuit”	7,145,374	12/05/06
D. Pang, F. Lin, P. Silverstri	“Power supply voltage detection circuitry and methods for use of the same”	7,148,742	12/12/06
F. Lin	“Delay-lock loop and method adapting itself to operate over a wide frequency range”	7,158,443	01/02/07
F. Lin	“Skew tolerant high-speed digital phase detector”	7,161,391	01/09/07
F. Lin	“System and method to improve the efficiency of synchronous mirror delays and delay locked loops”	7,161,399	01/09/07
F. Lin, B. Keeth, B. Johnson, SH. Lee	“Memory system and method for strobing data, command and address signals”	7,187,617	03/06/07
B. Johnson, F. Lin	“Duty cycle distortion compensation for the data output of a memory device”	7,206,956	04/17/07
F. Lin	“Measure-controlled delay circuits with reduced phase error”	7,208,986	04/24/07
F. Lin, B. Keeth	“Fast locking digital pahse locked loop”	7,221,201	05/22/07
SH. Lee, F. Lin	“Phase-locked loop circuits with reduced lock time”	7,230,495	06/12/07
F. Lin	“Circuits and methods of temperature compensation for refresh oscillator”	7,233,180	06/19/07
F. Lin, B. Keeth, B. Johnson, SH. Lee	“Memory system and method for strobing data, command and address signals”	7,245,553	07/17/07
F. Lin, B. Keeth, B. Johnson, SH. Lee	“Memory system and method for strobing data, command and address signals”	7,251,194	07/31/07
F. Lin, B. Johnson	“Method and apparatus for improving stability and lock time for synchronous circuits”	7,268,531	09/11/07
F. Lin, B. Keeth, B. Johnson, SH. Lee	“Memory system and method for strobing data, command and address signals”	7,269,094	09/11/07
F. Lin	“Method and apparatus to set a tuning range for an analog delay”	7,274,239	09/25/07
F. Lin	“Measure-controlled delay circuits with reduced phase error”	7,276,946	10/02/07
F. Lin	“Bias generator with feedback control”	7,282,972	10/16/07
F. Lin	“Circuits and methods of temperature compensation for refresh oscillator”	7,292,489	11/06/07
D. Pang, F. Lin, P. Silverstri	“Power supply voltage detection circuitry and methods for use of the same”	7,332,946	02/19/08
F. Lin	“Delay lock circuit having self-calibrating loop”	7,336,084	02/26/08
F. Lin, B. Keeth	“Fast locking digital pahse locked loop”	7,336,111	02/26/08
B. Johnson, F. Lin, B. Keeth	"Write latency tracking using a delay lock loop in a synchronous DRAM"	7,355,920	04/08/08

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Authors	Patent Title	#	Issued
B. Keeth, B. Johnson, F. Lin	“Method and apparatus for initialization of read latency tracking circuit in a high speed DRAM”	7,355,922	04/08/08
F. Lin, B. Johnson	“Method for improving stability and lock time for synchronous circuits”	7,420,361	09/02/08
F. Lin	“System and method to improve the efficiency of synchronous mirror delays and delay locked loops”	7,423,919	09/09/08
F. Lin	"Phase detector and method providing rapid locking of delay-locked loops"	7,428,284	09/23/08
F. Lin, B. Johnson	“Method and apparatus for calibrating driver impedance”	7,436,202	10/14/08
F. Lin	"Method and system for improved efficiency of synchronous mirror delays and delay locked loops"	7,443,743	10/28/08
F. Lin	"Loop filtering for fast PLL locking"	7,443,761	10/28/08
F. Lin	“System and method to improve the efficiency of synchronous mirror delays and delay locked loops”	7,446,580	11/04/08
F. Lin	“Bias generator with feedback control”	7,449,939	11/11/08
F. Lin	"Efficient clocking scheme for ultra high-speed systems"	7,454,646	11/18/08
F. Lin	“Phase detector for reducing noise”	7,463,099	12/09/08
B. Keeth, B. Johnson, F. Lin	“Method and apparatus for initialization of read latency tracking circuit in high-speed DRAM”	7,480,203	01/20/09
SH. Lee, F. Lin	"Clock signal distribution with reduced parasitic loading effects"	7,528,638	05/05/09
F. Lin	"Methods and apparatus for dividing a clock signal"	7,538,590	05/26/09
B. Johnson, F. Lin, B. Keeth	"Write latency tracking using a delay lock loop in a synchronous DRAM"	7,593,286	09/22/09
F. Lin	“System and method to improve the efficiency of synchronous mirror delays and delay locked loops”	7,605,620	10/20/09
F. Lin	“Delay-lock loop and method adapting itself to operate over a wide frequency range”	7,619,458	11/17/09
	subtotal	**79**	